Q. P Code: 21793

MUMBAI UNIVERSITY

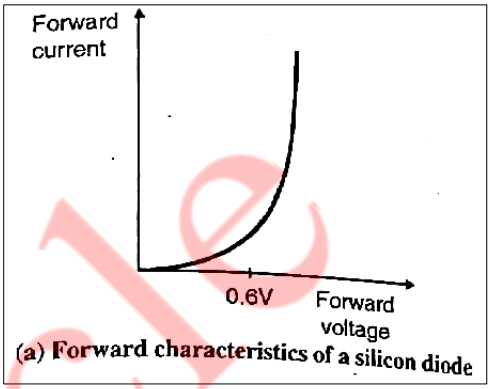
LINEAR INTEGRATED CIRCUITS (EXTC)

SEMESTER 4 – CBCGS – MAY 2018

Q.1 Attempt any 4 questions **20M**

(a) How precision rectifiers are different than simple diode rectifiers? **5M**

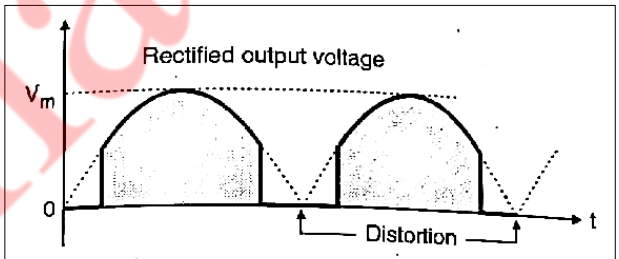
Ans. It is not possible to use the conventional rectifier circuits to rectify AC voltages below 0.3 or 0.6 Volts, because the minimum voltage required to forward bias a silicon diode is 0.6V.
The precision rectifiers will make it possible to rectify the AC input voltages of very small magnitudes, even less than 0.6 volts.



(a) Forward characteristics of a silicon diode

Problem with Basic Rectifiers and Need of Precision Rectifiers:
The forward characteristic of a diode is shown in **Fig.(a).**
It shows that the silicon diode requires 0.6v, to forward bias it.
Thus, for input signals having magnitudes less than 0.6V. the diode rectifier cannot be used.

A signal distortion is observed in the rectified output voltage as shown in **Fig.(b).**
even though the amplitude of input signal is higher than 0.6V.
The precision rectifiers are used for rectification of signals with small amplitudes, less than 0.6V.



(b) Distortion introduced in the rectifier output eventhough the input voltage is higher than 0.6 V

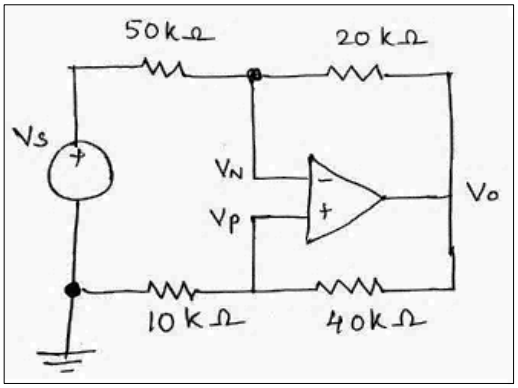
Types of precision rectifier:
1. Precision halfwave rectifier (HWR)
2. Precision full wave rectifier (FWR)

(b) Compare ideal op-amp with practical op-amp. **5M**

Ans.

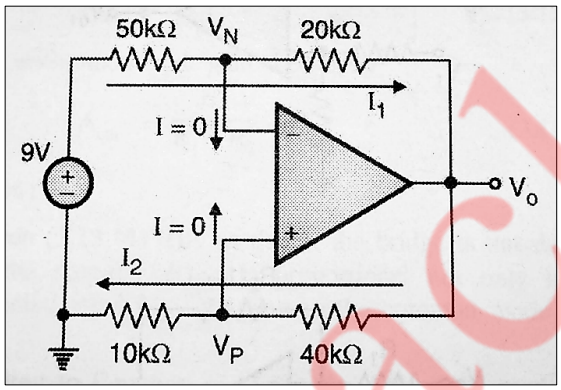
Sr. No.	Parameter	Symbol	Ideal op-amp.	Typical for 741 IC (practical op-amp.)
1	Open loop voltage gain	A_{OL}	∞	2×10^5
2	Output Impedance	Z_{out} or R_o	0	75 Ω
3	Input Impedance	Z_{in} or R_{in}	∞	2 MΩ
4	Input offset current	I_{ios}	0	6 nA
5	Input offset voltage	V_{ios}	0	2 mV
6	Bandwidth	B.W	∞	1 MHz
7	Common mode rejection ratio	CMRR	∞	90 dB
8	Slew rate	S	∞	0.5 V/μ
9	Input bias current	I_b	0	50 nA
10	Power supply rejection ratio	PSRR	0	150 μV/V

(c) Find V_N, V_P, and V_O in the circuit of Fig. l(c) if vs is 9V. **5M**



Ans. We assume that the OP-AMP is an ideal OP-AMP. Hence the input current for both the input terminals is zero and due to virtual short concept,

$$V_N = V_P$$



Step 1: Find Vo

From above fig. we get,

$$I_1 = \frac{9 - Vo}{70\ K\ \Omega}$$

$$V_N = 9 - 50\ K \times I_1 = 9 - \frac{50\ K(9 - V_o)}{70\ K\ \Omega} = \frac{63 - 45 + 5\ V_o}{7}$$

$$\therefore\ 7\ V_N = 18 + 5\ V_o \qquad \ldots(1)$$

$$\text{Also}\ \ I_2 = \frac{Vo}{50\ K}$$

$$\therefore\ V_P = 10\ K \times I_2 = \frac{V_o}{50} \times 10 = \frac{V_o}{5}$$

$$\text{But}\ V_N = V_P$$

$$\therefore \frac{18 + 5\ V_o}{7} = \frac{V_o}{5}$$

$$\therefore 90 + 25\ V_o = 7\ V_o$$

$$\therefore\ V_o = -5\ V$$

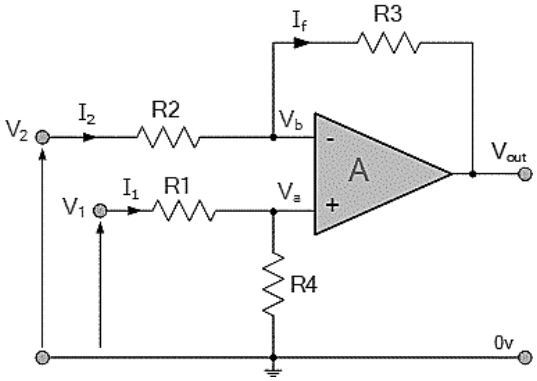
Step 2 : Find V_N and V_P

$$\therefore\ V_P = V_N = \frac{V_o}{5} = \frac{-5}{5} = -1V$$

Hence, $V_P = V_N = -1V$ and $V_o = -5\ V$

(d) Design a circuit for Vo = $2V_1$ - $3V_2$ using single op-amp and few resistors. **5M**

Ans. For the above output we have to use difference amplifier.



Expression for V_{02}

$$V_{02} = -\frac{R_F}{R_2} \times V_2$$

For $-3V_2$ Let R3 = R4 = R_F = 10KΩ

$$-3 = -\frac{R_F}{R_2}$$

$$R_2 = \frac{R_F}{3}$$

$$R_2 = \frac{10K}{3}$$

$$R_2 = 3.33K\Omega$$

Expression for V_{01}

$$V_{01} = A_{VF} \times V_a$$

$$V_{01} = \left[1 + \frac{R_F}{R_2}\right] \times \left[\frac{R_F}{R_F + R_1}\right] \times V_1$$

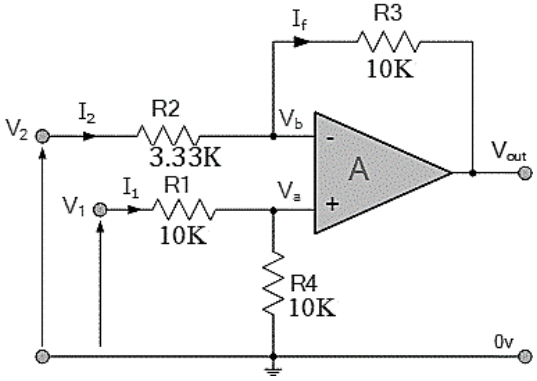
For $2V_1$

$$2 = \left[1 + \frac{R_F}{R_2}\right] \times \left[\frac{R_F}{R_F + R_1}\right]$$

$$2 = \left[1 + \frac{10K}{3.3K}\right] \times \left[\frac{10K}{10K + R_1}\right]$$

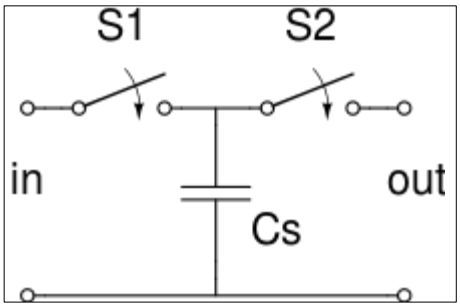
$$R_1 = 10K\Omega$$

So, the required resistor value is R3 = R4 = 10KΩ, R2 = 3.33KΩ, R1 = 10KΩ



(e) Explain how a resistor can be simulated by a switch capacitor circuit. **5M**

Ans. The simplest switched-capacitor (SC) circuit is the switched-capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge ***q*** from the input to the output at the switching frequency ***f***. The charge q on a capacitor C with a voltage V between the plates is given by: ***q = CV***



The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency (i.e., it is a programmable resistance).

The parasitic-sensitive integrator.

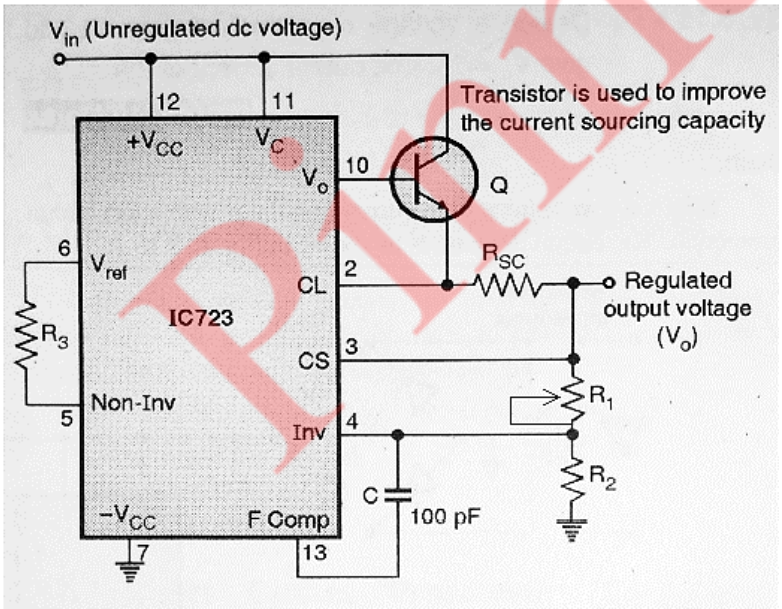
switched-capacitor circuits are used to provide accurate voltage gain and integration by switching a sampled capacitor onto an op-amp with a capacitor C_{fb} in feedback. One of the earliest of these circuits is the parasitic-sensitive integrator developed by the Czech engineer Bedrich Hosticka. Here is an analysis. Denote by $T=1/f$ the switching period. In capacitors,

charge = capacitance x voltage

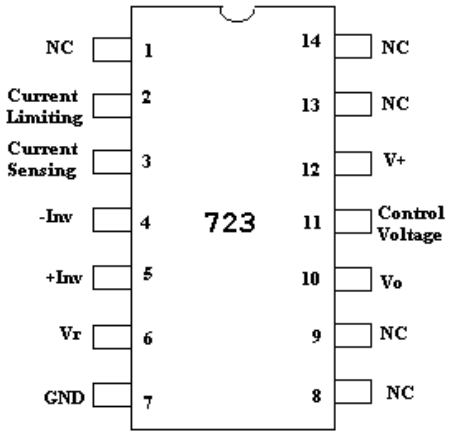
Q.2

(a) Design a voltage regulator using IC 723 to give Vo = 4V to 32V and output current of 2A. **10M**

Ans. The input unregulated voltage ranges from 9.5 to 40V and it can regulate voltage from 2V to 37V. It has an ability to provide up to 150 mA of current to the load, but this can be increased more than 10A by using power transistors.it can be used as either a linear or a switching regulator.



high voltage high current regulator



Pin diagram of IC 723

The IC's 723 is working on four application

1. LVLC (LOW VOLTAGE LOW CURRENT) – Range(2v-7v with 150mA)
2. LVHC (LOW VOLTAGE HIGH CURRENT) – Range(2v-7v with higher then 150mA)
3. HVLC (HIGH VOLTAGE LOW CURRENT) – Range(7v-37v with 150mA)
4. HVHC (HIGH VOLTAGE HIGH CURRENT) – Range(7v-37v with higher then 150mA)

So, it is not possible to regulate 4v to 32v using IC's 723.
We can regulate 7v to 32v with 2A current or 2v to 7v with 2A current

(b) Explain R-2R ladder type digital to analog convertor. **10M**

Ans. This is the second type of resistive network used for the D to A conversion.
It consists of resistors of only two values, R and 2R.
the R-2R network is the heart of R-2R ladder type DAC and the one is a 4-bit R-2R network. shown fig.1

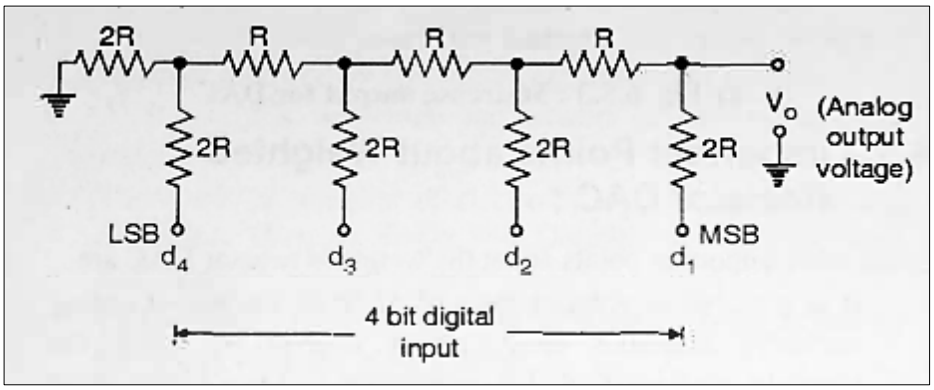


Fig.1 4-bit R-2R ladder network

d_1 d_2 d_3 d_4 is a 4-bit digital input word with d_1 as the Most Significant Bit (MSB) and d_4 as the Least Significant Bit (LSB).
V_O is the analog output voltage which is proportional to the digital input.
The R-2R network can be analysed by using the Thevenin's theorem.
While analysing, we will obtain the output voltage corresponding to each digital input d_1 d_2 d_3 or d_4 separately and then add them to get the final value of V_O.
The principle of superposition can be applied to this network because this is a linear network.

The results of analysis have been in Table.

Digital input			Output voltage	
d_1 MSB	d_2	d_3	d_4 LSB	V_O Volts
0	0	0	1	$V_R/16$
0	0	1	0	$V_R/8$
0	1	0	0	$V_R/4$
1	0	0	0	$V_R/2$

the expression for the analog output voltage is,

$$Vo = V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}]$$

It is possible to have a 2-bit, 3-bit, 5-bit or n-bit R-2R ladder.
The problem of using a wide range of resistor values (for weighted resistor DAC) can be solved by using the R-2R ladder type DAC.
The circuit diagram for R-2R ladder type DAC is shown in fig.2 It shows that only two values of resistors are required namely R Ω and 2 R Ω.
This method is therefore suitable for the realization of Integrated Circuits (IC). The value of R in Fig.2 can be anywhere between 2.5 k Ω to 10 k Ω but it should not be less than 2.5k Ω.

Operation of R-2R ladder DAC

the number of digits per binary word is assumed to be 3 (i.e. n = 3). The switch position indicate that the binary word is d_1 d_2 d_3 = l00.
The original circuit can now be simplified as shown in Figs.3 and 4 respectively.
The simplified circuit shown in Fig.3 gets further reduced to the simplified equivalent circuit shown in Fig. 6.6.4. The equivalent resistance to the left of node ''B'' in Fig. 6.6.3 is only ''2R'' and node A is at ''virtual ground'' potential.

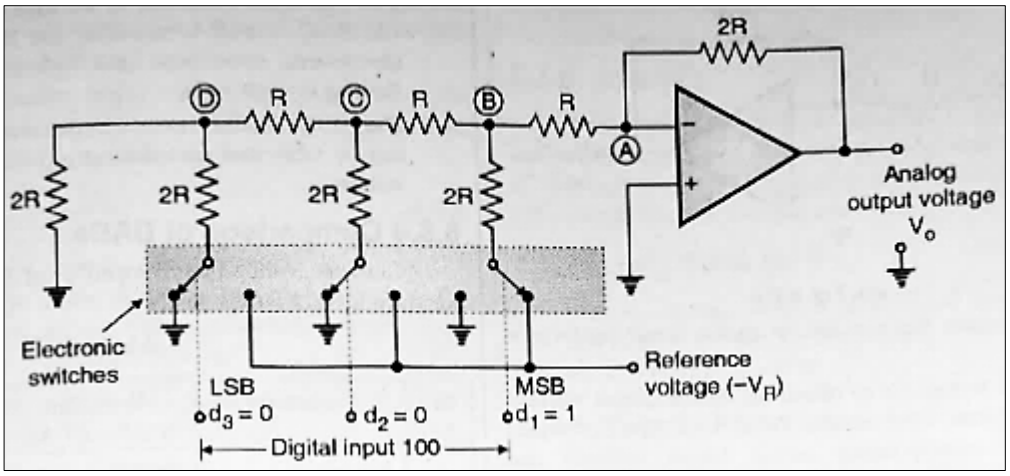


Fig.2 : R-2R ladder DAC

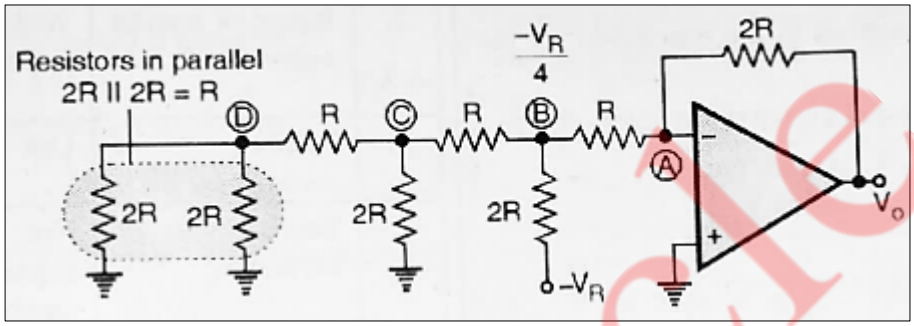
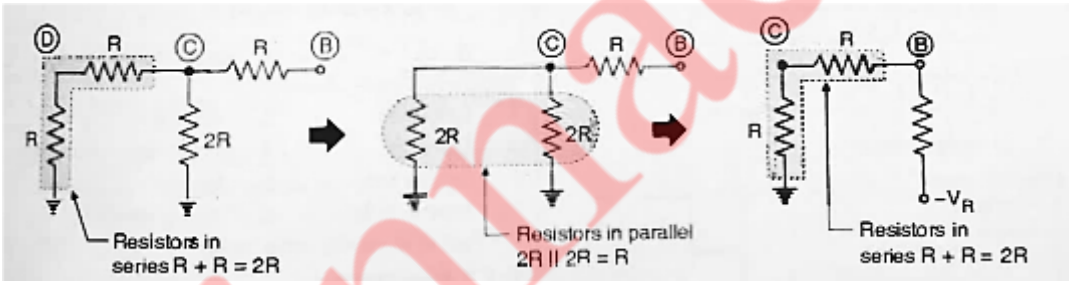
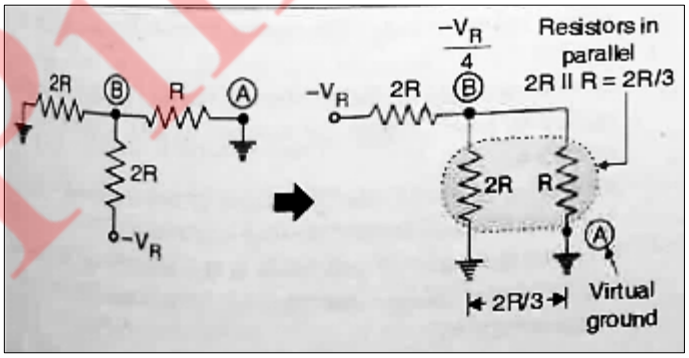


Fig.3 : Simplified R-2R ladder DAC



Simplified equivalent circuits to the left of B.



(a) simplified equivalent circuit. (b) Final equivalent circuit

The simplified equivalent circuit of Fig.(a) is redrawn as shown in Fig(b). As the two resistors Rand 2R are in parallel with each other, their parallel combination results in a resistance of (2 R/3) Ω. voltage at node B is given by,

$$V_B = \frac{(2R/3)}{2R + (2R/3)} \times (-V_R)$$

$$V_B = \frac{(2R/3)}{\left[\frac{6R + 2R}{3}\right]} \times (-V_R)$$

$$V_B = \frac{-V_R}{4}$$

Considering the OP-AMP to be an inverting amplifier the equivalent circuit of the DAC is as shown in Fig.4

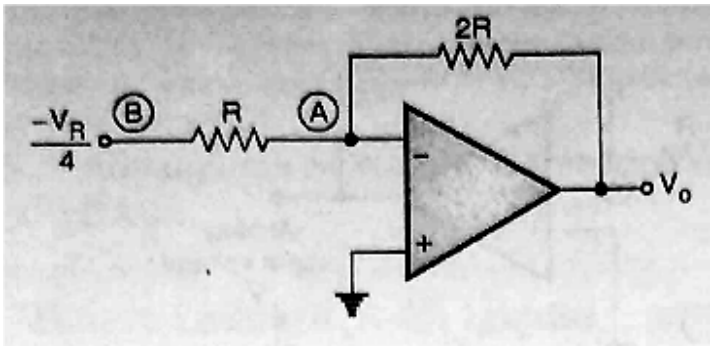


Fig.4

Hence the output voltage is given by,

$$V_O = \left[\frac{-R_F}{R_i}\right] \times V_{in} = \frac{-2R}{R} \times \frac{-V_R}{4}$$

$$V_O = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

Thus, for a binary input of 100 the analog output produced is $V_R/2$.
Similarly, it is possible to obtain the analog output voltages for other digital input words. In table lists the digital inputs and corresponding analog output voltages and Fig. 5 shows the staircase output voltage waveform obtained for R-2R ladder DAC.
Note- that this is exactly identical to the one drawn for the weighted resistor DAC.

Digital input			Analog output voltage V_O
d1	d2	d3	
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2\ V_R/8$
0	1	1	$3\ V_R/8$
1	0	0	$4\ V_R/8$
1	0	1	$5\ V_R/8$
1	1	0	$6\ V_R/8$
1	1	1	$7\ V_R/8$

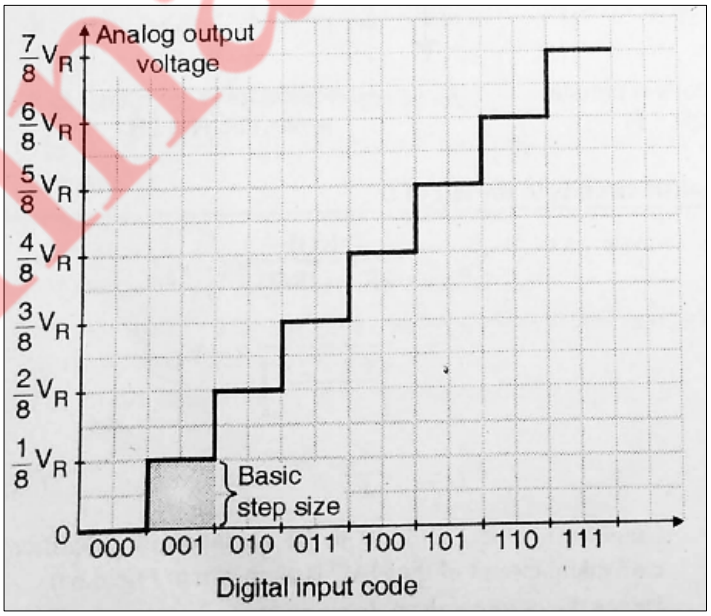


Fig.1 staircase analog output voltage for R-2R ladder DAC

Advantages of R/2R Ladder DACs:

1. Because we need resistors of only two values (R and 2 R), it is easier to build this circuit accurately.

2. We can increase the number of input bits just by adding more sections of same R/2R values.

3. The equivalent resistance to the right of each labelled node (A, B, C) will be equal to 2R. Hence current flowing downwards, away from each node is equal to the current flowing towards right.

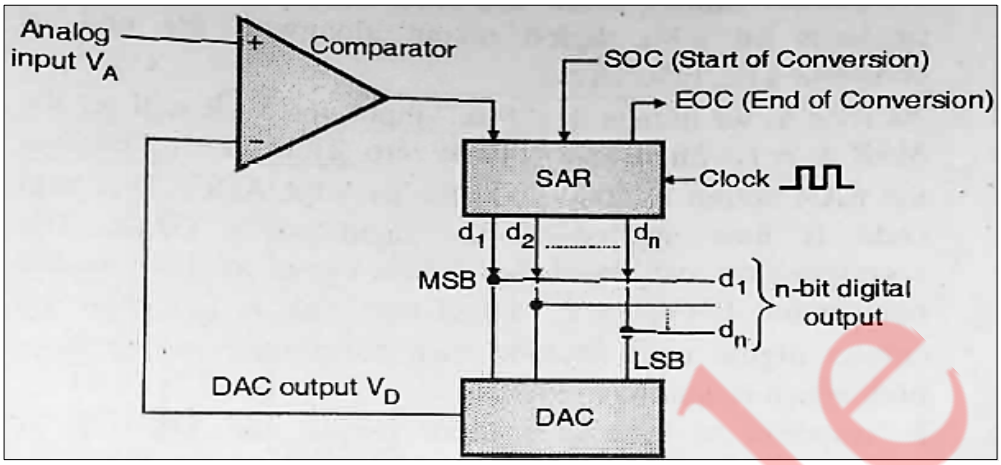
4. Due to the small resistance range required, the R-2R ladder can be fabricated monolithically, with a high accuracy and stability.

Q.3

(a) Explain analog to digital conversion using successive approximation method. **10M**

Ans. Successive approximation ADC is one of the most widely and popularly used ADC technique.
The ADC operation is based upon an efficient "code search" strategy to complete the n-bit conversion in just n-clock periods.
Thus, it takes much shorter conversion time as compared to the counter type ADC.

Block diagram:



Successive approximation ADC

1. **Initially : SAR output : d_1 .....d_8 = 0000 0000**
   $\therefore$ $V_D = 0$ $\therefore$ Comparator output = 1
   $\therefore$ Bit d_1 is made 1
2. **New SAR output : d_1 .... d_8 = 1000 0000.**
   Compare V_D with V_A.
   $V_D < V_A$ $\therefore$ Comparator output = 1
   $\therefore$ Make bit $d_2 = 1$.
3. **New SAR output : d_1 .... d_8 = 1100 0000**
   Compare V_D with V_A
   $V_D < V_A$ $\therefore$ Comparator output = 1.
   Make bit $d_3 = 1$.
4. **New SAR output : d_1 ..... d_8 = 1110 0000**
   Compare V_D with V_A
   $V_D > V_A$ $\therefore$ Comparator output = 0.
   So make $d_3 = 0$ and $d_4 = 1$
5. **New SAR output : d_1 ..... d_8 = 1101 0000**
   Compare V_D with V_A.
   $V_D < V_A$. $\therefore$ Comparator output = 0.
   So make $d_5 = 1$
6. **New SAR output : d_1 ..... d_8 = 1101 1000**
   Continue the same process as follows.

SAR output								Comparator output
d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8	
1	1	0	1	1	0	0	0	$V_D > V_A$ → 0
1	1	0	1	0	1	0	0	$V_D > V_A$ → 0
1	1	0	1	0	0	1	0	Stop as $V_D = V_A$

Make $d_5 = 0$ and $d_6 = 1$

Make $d_6 = 0$ and $d_7 = 1$

Operation:

1. The successive approximation register SAR receives the comparator output, clock and start conversion signals and produces an n-bit digital output along with the end of conversion i.e. EOC signal.
2. As soon as we initiate the "SOC" input, the SAR will set the MSB $d_1 = 1$. with all other bits to zero. Thus, the trial code at the SAR output is 1000 0000 for an 8-bit ADC. This trial code is then applied at the input of a DAC. The corresponding output of DAC i.e. V_D is applied to the comparator. If ($V_D < V_A$) i.e. if trial code is less than the correct digital representation then comparator output goes high which is applied to SAR.
3. In response to high comparator output, the MSB d_1 is maintained at "1" and the next lower significant bit d_2 is made "1". The trial code at the SAR output now becomes 1100 0000. The corresponding DAC output is compared with V_A and the process continues as explained in 2.
4. However, for the first trial code of 1000 0000 only if $V_A < V_D$, then the comparator output will go low i.e. 0. The SAR will respond to it by resetting its MSB bit d_1 to 0 and making the next bit $d_2 = 1$ so that the new trial code is 0100 0000.
5. This procedure is repeated for all the subsequent bits one at a time, until all bit positions are tested.
6. As soon as the DAC output V_D crosses V_A (i.e. $V_D > V_A$), the comparator changes state and this is taken as End of Conversion (EOC) command.

Suppose that for the given analog input voltage the correct digital output is 1101 0010. Then the SAC ADC reaches this word in the way for $V_A \geq V_D$ the comparator output becomes high and for $V_A < V_D$ the comparator output is low.

Advantages:

1. The conversion time is equal to the 'n' clock cycle period for an n-bit ADC. Thus, conversion time is very short. For example, for a 10-bit ADC with a clock frequency of 1Mhz, the conversion time will be 10x10^-6 i.e. 10 µsec only.
2. Conversion time is constant and independent of the amplitude of analog signal V_A.

Disadvantages:

1. The circuit is complex.
2. The conversion time is longer as compared to flash type ADC.

Applications:

Due to the advantages mentioned earlier the successive approximation ADC is most widely used in the microprocessor-based data acquisition systems. IC ADC 0809 uses the concept of successive approximation.

(b) Draw a neat circuit diagram of a RC phase shift oscillator using op-amp. Derive its frequency of oscillation. What are the values of R and C for frequency of oscillation to be 1 kHz? 10M

Ans. 1. Given that frequency of oscillations, $f_O = 1$ kHz.
Assume, C = 0.01 µF, to calculate R.

$$\because \ fo = \frac{1}{2\pi\sqrt{6}\,RC}$$

$$\therefore \ R = \frac{1}{2\pi\sqrt{6}\,foC} = \frac{1}{2\pi\sqrt{6} \times 1 \times 10^{3} \times 0.01 \times 10^{-6}}$$

$$R = 6.497\ K\Omega \approx 6.5\ K\Omega$$

2. For sustained oscillations, the gain of the inverting amplifier should be at least 29.

$$\therefore \ |A| \geq 29$$

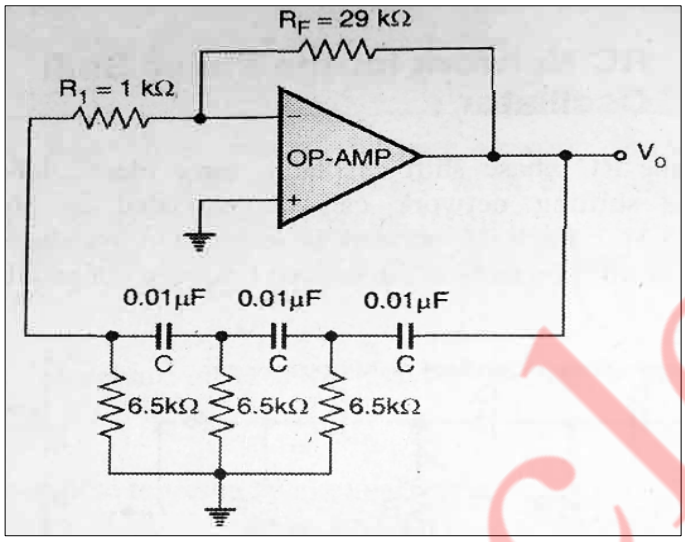
$$\text{But} \quad |A| = \frac{Rf}{R1}$$

$$\therefore \left|\frac{Rf}{R1}\right| \geq 29$$

Let R1 = 1 KΩ

$\therefore R_F = 29$ KΩ

The required R-C phase shift oscillator is shown fig

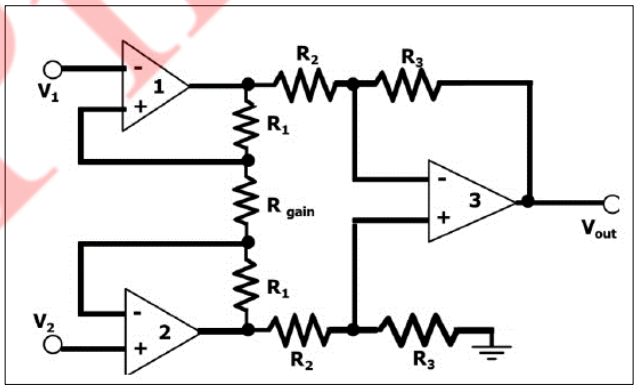


Q.4

(a) What is an instrumentation amplifier? Draw a neat circuit of an instrumentation amplifier using 3 op-amps. Derive its output voltage equation. **10M**

Ans. An instrumentation amplifier is used to amplify very low-level signals, rejecting noise and interference signals.

The op-amps 1 & 2 are non-inverting amplifiers and op-amp 3 is a difference amplifier. These three op-amps together, form an instrumentation amplifier. Instrumentation amplifier's final output Vout is the amplified difference of the input signals applied to the input terminals of op-amp 3. Let the outputs of op-amp 1 and op-amp 2 be Vo1 and Vo2 respectively.



The three OP-AMP instrumentation amplifier

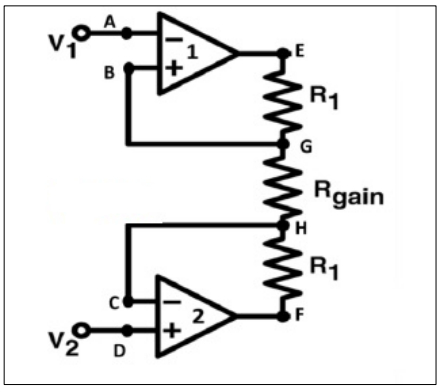
Then, Vout = (R3/R2) (Vo1-Vo2)

Look at the input stage of the instrumentation amplifier as shown in the figure below.

The instrumentation amplifier derivation is discussed below.

The potential at node A is the input voltage V1. Hence the potential at node B is also V1, from the virtual short concept. Thus, the potential at node G is also V1.

The potential at node D is the input voltage V2. Hence the potential at node C is also V2, from the virtual short. Thus, the potential at node H is also V2.



Input Stage of the Instrumentation Amplifier

The working of the instrumentation amplifier is, Ideally the current to the input stage op-amps is zero. Therefore, the current I through the resistors R1, Rgain, and R1 remain the same.

Applying Ohm's law between nodes E and F,

I = (Vo1-Vo2)/(R1+Rgain+R1) ……(1)
I = (Vo1-Vo2)/(2R1+Rgain)

Since no current is flowing to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

I = (VG-VH) / Rgain = (V1-V2) / Rgain……(2)

Equating equations 1 and 2,

(Vo1-Vo2)/(2R1+Rgain) = (V1-V2)/Rgain
(Vo1-Vo2) = (2R1+Rgain)(V1-V2)/Rgain ……(3)

The output of the difference amplifier is given as,

Vout = (R3/R2) (Vo1-Vo2)

Therefore, (Vo1 – Vo2) = (R2/R3)Vout

Substituting (Vo1 – Vo2) value in equation 3,

we get (R2/R3)Vout = (2R1+Rgain)(V1-V2)/Rgain

i.e. Vout = (R3/R2){(2R1+Rgain)/Rgain}(V1-V2)

This above equation gives the output voltage of an instrumentation amplifier.
The overall gain of the amplifier is given by the term (R3/R2){(2R1+Rgain)/Rgain}.
The overall voltage gain of an instrumentation amplifier can be controlled by adjusting the value of resistor Rgain.
The common mode signal attenuation for the instrumentation amplifier is provided by the difference amplifier.

Advantages of the instrumentation amplifier.

- The gain of a three op-amp instrumentation amplifier circuit can be easily varied by adjusting the value of only one resistor Rgain.
- The gain of the amplifier depends only on the external resistors used.
- The input impedance is very high due to the emitter follower configurations of amplifiers 1 and 2
- The output impedance of the instrumentation amplifier is very low due to the difference amplifier3.

- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

Applications of Instrumentation Amplifier.

- Instrumentation amplifiers are used in data acquisition from small o/p transducers like thermocouples, strain gauges, measurements of Wheatstone bridge, etc.
- These amplifiers are used in navigation, medical, radar, etc.
- These amplifiers are used to enhance the S/N ratio (signal to noise) in audio applications like audio signals with low amplitude.
- These amplifiers are used for imaging as well as video data acquisition in the conditioning of high-speed signal.
- These amplifiers are used in RF cable systems for amplification of the high-frequency signal.

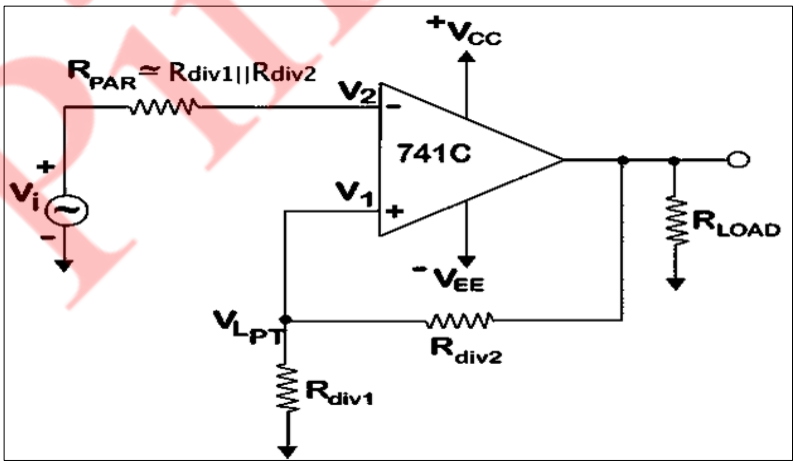
Important features of an instrumentation amplifier are as follows:

a. High CMRR (Common Mode Rejection Ratio)
b. Large input impedance.
c. Low output impedance.
d. High gain accuracy.
e. Both the input voltage should not be same i.e. $V_1 \neq V_2$.
f. High gain stability with low temperature coefficient.

(b) With the help of a neat diagram and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expressions for its threshold levels. **10M**

Ans. A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages.

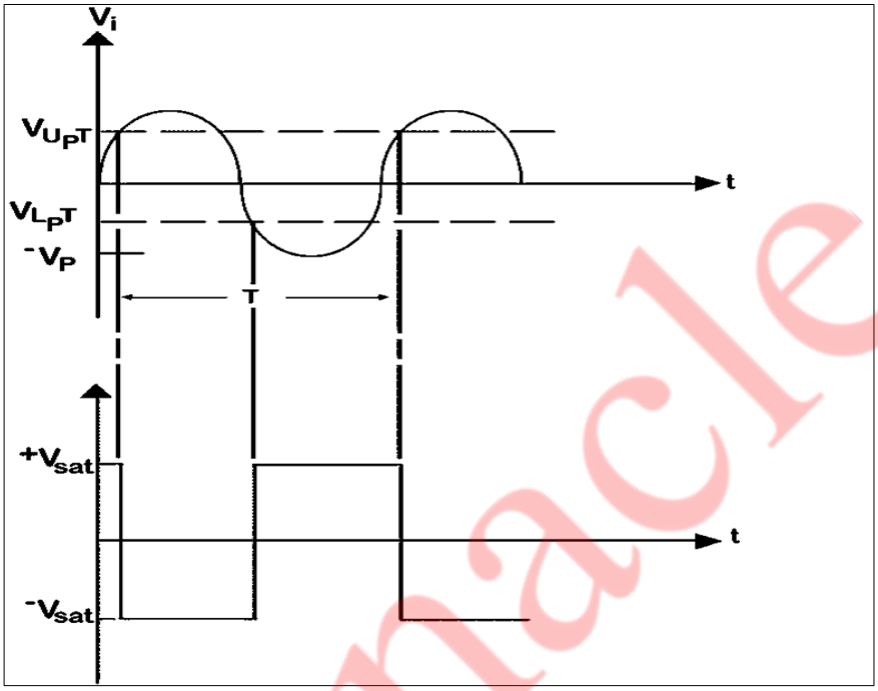
the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit.



Schmitt Trigger using Op-Amp

in the circuit diagram, a voltage divider with resistors Rdiv1 and Rdiv2 is set in the positive feedback of the 741 IC op-amp. The same values of Rdiv1 and Rdiv2 are used to get the resistance value Rpar = Rdiv1||Rdiv2 which is connected in series with the input voltage. Rpar is used to minimize the offset problems. The voltage across R1 is feedback to the non-inverting input. The input voltage Vi triggers or changes the state of output Vout every time it exceeds its voltage levels above a certain threshold value called Upper Threshold Voltage (Vupt) and Lower Threshold Voltage (Vlpt).

Let us assume that the inverting input voltage has a slight positive value. This will cause a negative value in the output. This negative voltage is feedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the negative voltage that is feedback to the positive terminal becomes higher. The value of the negative voltage becomes again higher until the circuit is driven into negative saturation (-Vsat). Now, let us assume that the inverting input voltage has a slight negative value. This will cause a positive value in the output. This positive voltage is feedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the positive voltage that is feedback to the positive terminal becomes higher. The value of the positive voltage becomes again higher until the circuit is driven into positive saturation (+Vsat). This is why the circuit is also named a regenerative comparator circuit.



Input and Output Waveform

When Vout = +Vsat, the voltage across Rdiv1 is called Upper Threshold Voltage (Vupt). The input voltage, Vin must be slightly more positive than Vupt in order to cause the output Vo to switch from +Vsat to -Vsat. When the input voltage is less than Vupt, the output voltage Vout is at +Vsat.

Upper Threshold Voltage, Vupt = +Vsat (Rdiv1/[Rdiv1+Rdiv2])

When Vout = -Vsat, the voltage across Rdiv1 is called Lower Threshold Voltage (Vlpt). The input voltage, Vin must be slightly more negative than Vlpt in order to cause the output Vo to switch from -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat.

Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[Rdiv1+Rdiv2])

If the value of Vupt and Vlpt are higher than the input noise voltage, the positive feedback will eliminate the false output transitions. With the help of positive feedback and its regenerative behaviour, the output voltage will switch fast between the positive and negative saturation voltages.

Voltage transfer characteristics

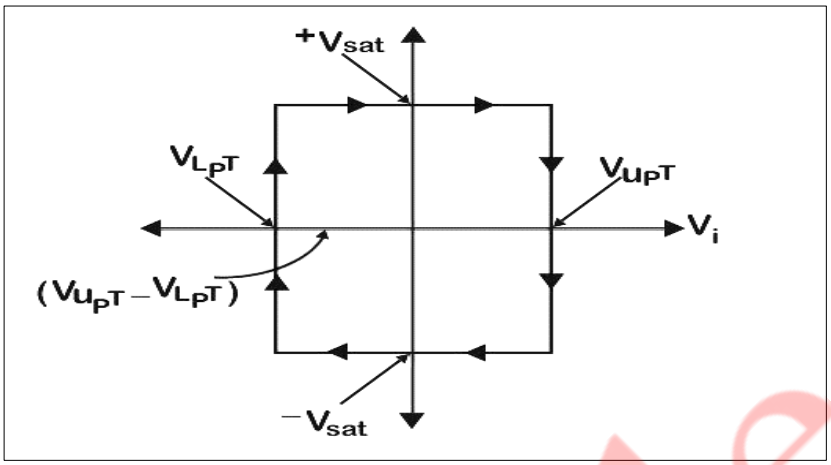
Since a comparator circuit with a positive feedback is used, a dead band condition hysteresis can occur in the output. When the input of the comparator has a value higher than Vupt, its output switches from +Vsat to -Vsat and reverts back to its original state, +Vsat, when the input value goes below Vlpt. This is shown in the figure below. The hysteresis voltage can be calculated as the difference between the upper and lower threshold voltages.

Vhysteresis = Vupt – Vlpt

Substituting the values of Vupt and Vlpt from the above equations:

Vhysteresis = +Vsat (Rdiv1/Rdiv1+Rdiv2) – {-Vsat (Rdiv1/Rdiv1+Rdiv2)}

Vhysteresis = (Rdiv1/Rdiv1+Rdiv2) {+Vsat – (-Vsat)}



Input - Output Characteristics
Hysteresis Voltage Plot

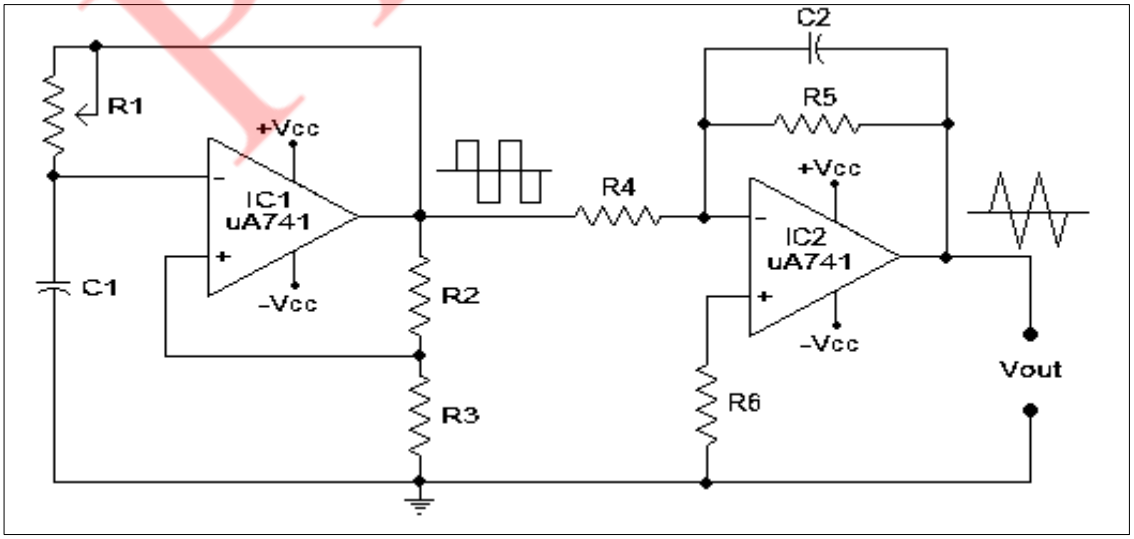
Applications of Schmitt Trigger

- Analog to digital conversion: The Schmitt trigger is effectively a one-bit analog to digital converter. When the signal reaches a given level, it switches from its low to high state.
- Level detection: The Schmitt trigger circuit is able to provide level detection. When undertaking this application, it is necessary that the hysteresis voltage is taken into account so that the circuit switches on the required voltage.
- Line reception: When running a data line that may have picked up noise into a logic gate it is necessary to ensure that a logic output level is only changed as the data changed and not as a result of spurious noise that may have been picked up. Using a Schmitt trigger broadly enables the peak to peak noise to reach the level of the hysteresis before spurious triggering may occur.

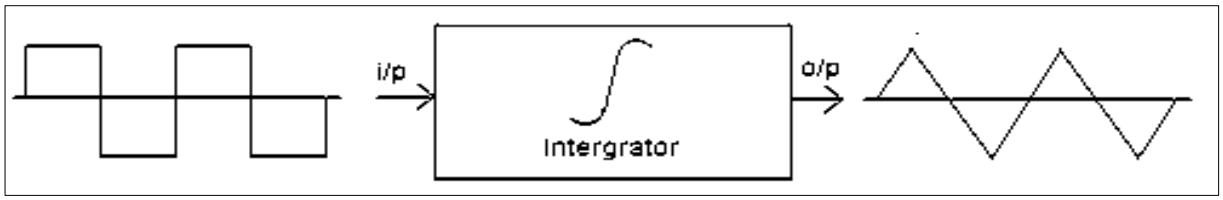
Q.5

(a) Draw the circuit diagram of a square and triangular waveform generator using op-amp and explain its working with the help of waveforms. **10M**

Ans. This circuit is based on the fact that a square wave on integration gives a triangular wave.



Triangular waves are a periodic, non-sinusoidal waveform with a triangular shape.



Generating triangular wave from a square wave

To generate triangular waves, we need an input wave. we are using square waves for input. square waves have equal rise and fall times so they are more convenient to be converted to a triangular waveform.

Square wave generator

The square wave generator is based on a uA741 op-amp (IC1). Resistor R1 and capacitor C1 determines the frequency of the square wave. Resistor R2 and R3 forms a voltage divider setup which feedbacks a fixed fraction of the output to the non-inverting input of the IC.

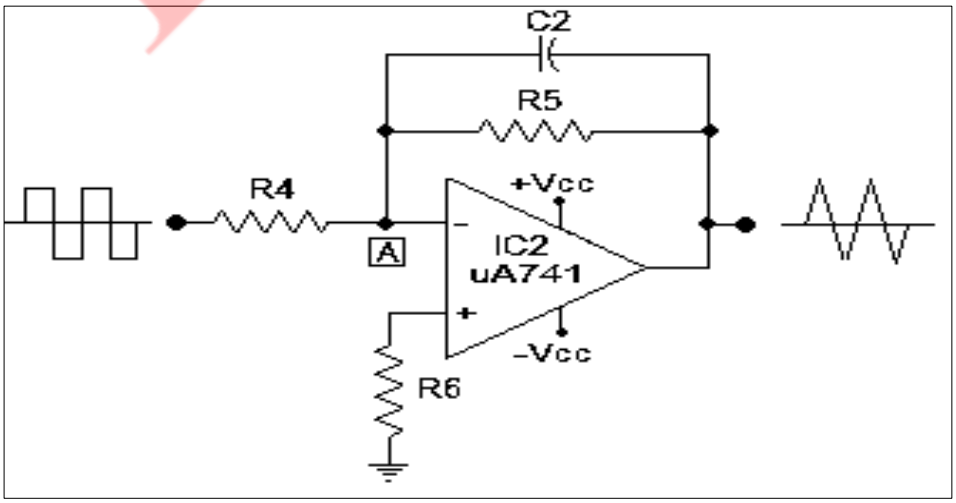
Initially, when power is not applied the voltage across the capacitor C1 is 0. When the power supply is switched ON, the C1 starts charging through the resistor R1 and the output of the op-amp will be high (+Vcc). A fraction of this high voltage is fed back to the non- inverting pin by the resistor network R2, R3. When the voltage across the charging capacitor is increased to a point the voltage at the inverting pin is higher than the non-inverting pin, the output of the op-amp swings to negative saturation (-Vcc). The capacitor quickly discharges through R1 and starts charging in the negative direction again through R1. Now a fraction of the negative high output (-Vcc) is fed back to the non-inverting pin by the feedback network R2, R3. When the voltage across the capacitor has become so negative that the voltage at the inverting pin is less than the voltage at the non-inverting pin, the output of the op-amp swings back to the positive saturation. Now the capacitor discharges trough R1 and starts charging in positive direction. This cycle is repeated over time and the result is a square wave swinging between +Vcc and -Vcc at the output of the op-amp.

If the values of R2 and R3 are made equal, then the frequency of the square wave can be expressed using the following equation:

$$F=1 / (2.1976 R1C1)$$

Integrator

Next part of the triangular wave generator is the op-amp integrator. Instead of using a simple passive RC integrator, an active integrator based on op-amp is used here. The op-amp IC used in this stage is also uA741 (IC2). Resistor R5 in conjunction with R4 sets the gain of the integrator and resistor R5 in conjunction with C2 sets the bandwidth. The square wave signal is applied to the inverting input of the op-amp through the input resistor R4. The op-amp integrator part of the circuit is shown in the figure below.



Let's assume the positive side of the square wave is first applied to the integrator. By virtue, capacitor C2 offers very low resistance to this sudden shoot in the input and C2 behaves something like a short circuit. The feedback resistor R5 connected in parallel to C2 can be put aside because R5 has almost zero resistance at the moment. A serious amount of current flows through the input resistor R4 and the capacitor C2 bypasses all these current. As a result, the inverting input terminal (tagged A) of the op-amp behaves like a virtual ground because all the current flowing into it is drained by the capacitor C2. The gain of the entire circuit (Xc2/R4) will be very low and the entire voltage gain of the circuit will be close to the zero.

After this initial "kick" the capacitor starts charging and it creates an opposition to the input current flowing through the input resistor R4. The negative feedback compels the op-amp to produce a voltage at its out so that it maintains the virtual ground at the inverting input. Since the capacitor is charging its impedance Xc keeps increasing and the gain Xc2/R4 also keeps increasing. This results in a ramp at the output of the op-amp that increases in a rate proportional to the RC time constant **(T=R4C2)** and this ramp increases in amplitude until the capacitor is fully charged.

When the input to the integrator (square wave) falls to the negative peak the capacitor quickly discharges through the input resistor R4 and starts charging in the opposite polarity. Now the conditions are reversed and the output of the op-amp will be a ramp that is going to the negative side at a rate proportional to the R4R2 time constant.

This cycle is repeated and the result will be a triangular waveform at the output of the op-amp integrator.

Applications:

The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc.

(b) Analyze the circuit, Draw the waveforms at output terminal V_O and across the capacitor C. Comment on the duty cycle of output waveform. Take diode D as an ideal diode and assume R_A is equal to R_B. **10M**

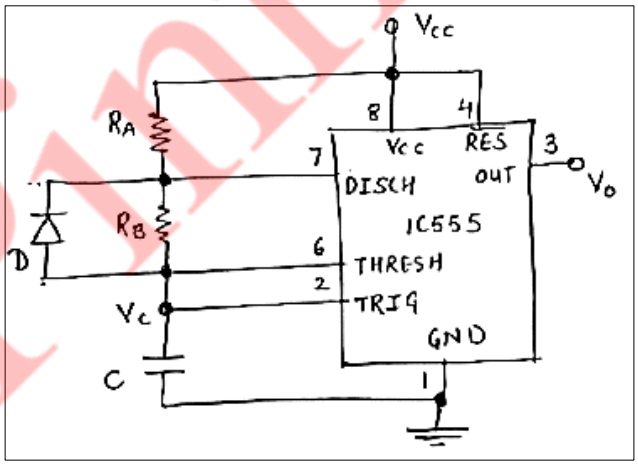


Fig. 1

Ans. **Note for students in tech-max the diode position is reverse.**

The circuit is basically in astable multivibrator mode. Here, while charging the capacitor, capacitor charges through RA and RB (since diode D is connected reverse).

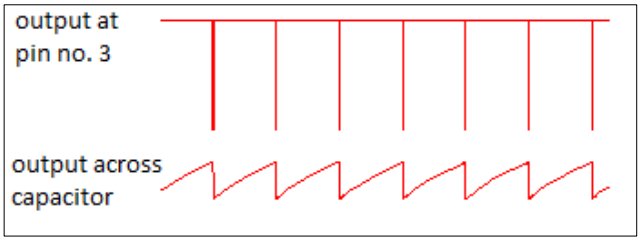
Thus, $T_C = 0.694(R_B+R_A)*C$.

While discharging, the capacitor will discharge through diode D (since diode D is ideal, offers zero resistance).

Thus, $T_d = 0.694\ Ro*C = 0$.

Therefore, Duty cycle $= \frac{T_c}{T_c + T_d} = 100\%$ (approximately) provided ON resistance of internal transistor connected to discharge pin 7 is zero.)

Appropriate waveforms are shown below.



Output Waveforms

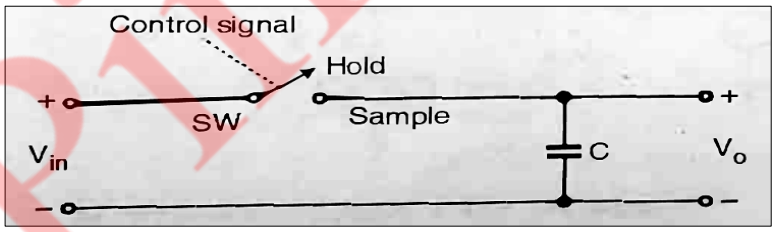
Q.6 Short notes on: (Attempt any four).

(a) Sample and hold circuit. **5M**

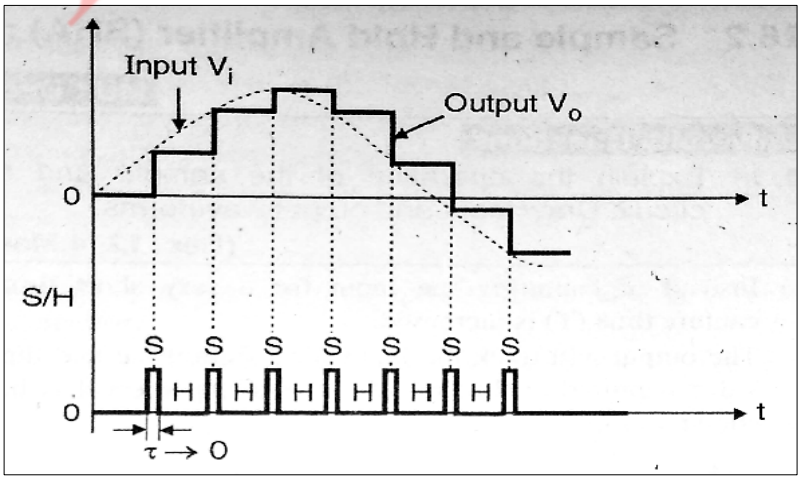
Ans. The basic sample and hold circuit shown in Fig. has one input, one output and an electronic switch which can be controlled by a control signal. The electronic switch can be a device such as a BJT or MOSFET which is biased to operate as a switch.
There are two possible modes of operation namely sampling mode and hold mode depending on the position of the switch.

Sampling mode:
In this mode, the switch is in the closed position and the capacitor charges to the instantaneous input voltage. This is sampling process.

Hold mode:
In this mode, this switch is in the "open" position. The capacitor is now disconnected from the input.
As there is no path for the capacitor to discharge, it will hold the voltage which was present across it just before opening the switch.
The capacitor will hold this voltage till the next sampling instant.



Basic sample and hold circuit

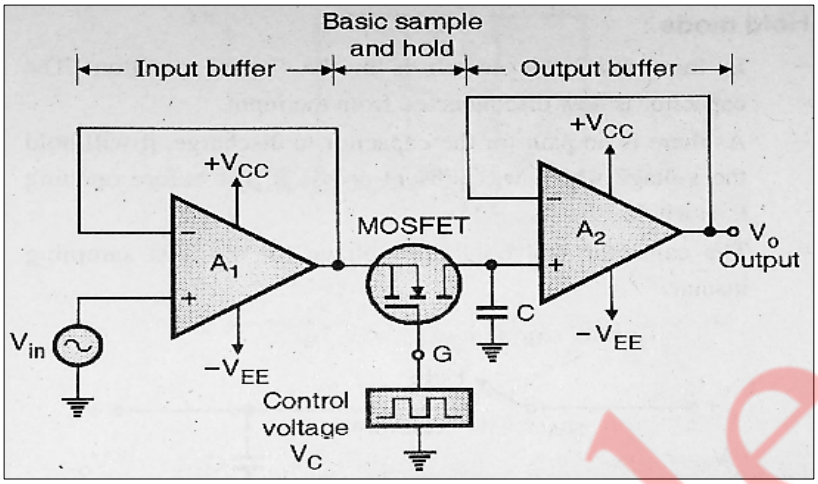


Response of a sample and hold amplifier.

or

Sample and Hold Circuit using OP-AMP:

Then-channel MOSFET which acts as a switch is driven by a control voltage Vc. It controls voltage Vc is applied to the gate of the MOSFET.



Sample and hold circuit using OP-AMP

Operation of the circuit:

The circuit diagram is split into three stages:

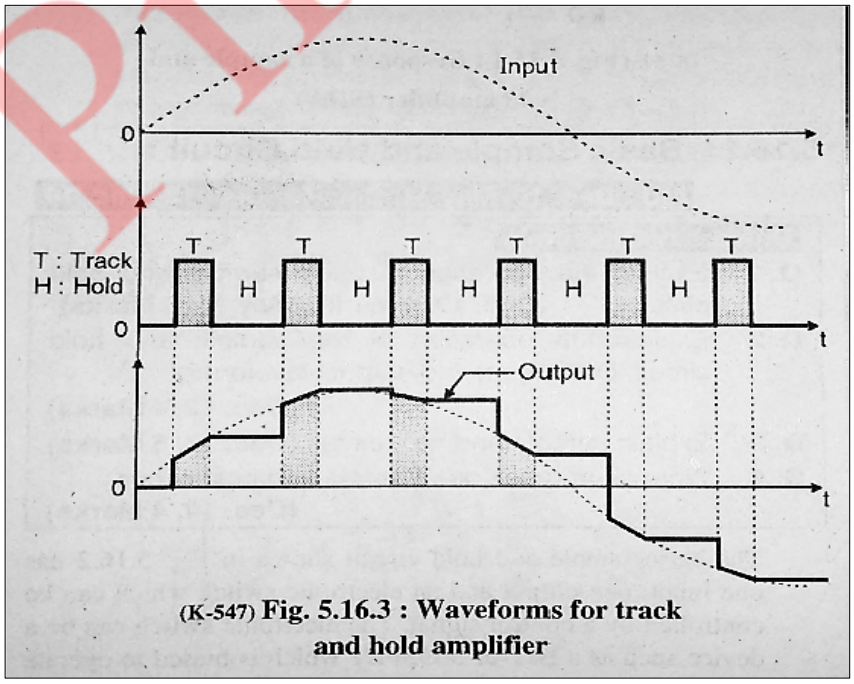
First stage is the voltage follower, second one is the switch and capacitor and the third one is again the voltage follower. The first voltage follower (buffer) A_1 is used in order to avoid the loading of input source V_{in} whereas the second buffer A2 ensures that the capacitor is not loaded.

When Vc is high, the MOSFET turns on and acts like a closed switch. This is sampling mode. The capacitor charges through the MOSFET to the instantaneous input voltage.

As soon as Vc = 0, the MOSFET turns off and the capacitor is disconnected from OP-AMP A_1 output.

Capacitor cannot discharge through amplifier A_2 due to its high input impedance.

Thus, this is the hold mode in which the capacitor holds the latest sample value. Waveform for both these modes have been shown in Fig.



(K-547) **Fig. 5.16.3 : Waveforms for track and hold amplifier**

Waveforms for track and hold amplifier

Precautions:

The total period T = T_H + T_S as shown in Fig. where TH = Holding time and Ts = Sampling time.
This total period should be at least half of one cycle period of the input signal. In other words, frequency of Vc should be at least twice the frequency of Vin.
The capacitor C should be leak proof. We can use the polyester or Teflon capacitors.

Applications of sample and hold circuit:

1. In the Pulse Modulation Systems.
2. In the Ana1og to Digital Converter (ADC).
3. In digital interfacing.
4. In the analog demultiplexers.

(b) Three terminal fixed voltage regulators. **5M**

Ans. the three terminal voltage regulators are of two types, namely, fixed voltage regulators and adjustable voltage regulators.
In the fixed voltage regulator category, we have positive voltage regulators and negative output voltage regulators.
The IC's 78XX series is a series of fixed positive voltage regulators and IC's 79XX is the series of fixed negative voltage regulators.

78XX Series (Fixed Positive Voltage Regulator):
78XX series are three terminal, positive fixed voltage regulators. Here XX indicate the output voltage.
These regulators are available in seven different output voltage options, such as 5, 6, 8, 12, 15, 18 and 24.
Thus, if we select a regulator IC numbered "7812'", it provides us a 12 V regulated output voltage.

IC No.	7805	7806	7808	7812	7815	7818	7824
Output voltage	5V	6V	8V	12V	15V	18V	24V

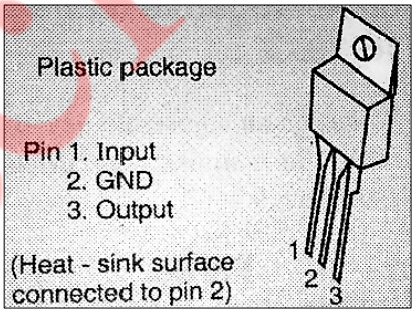
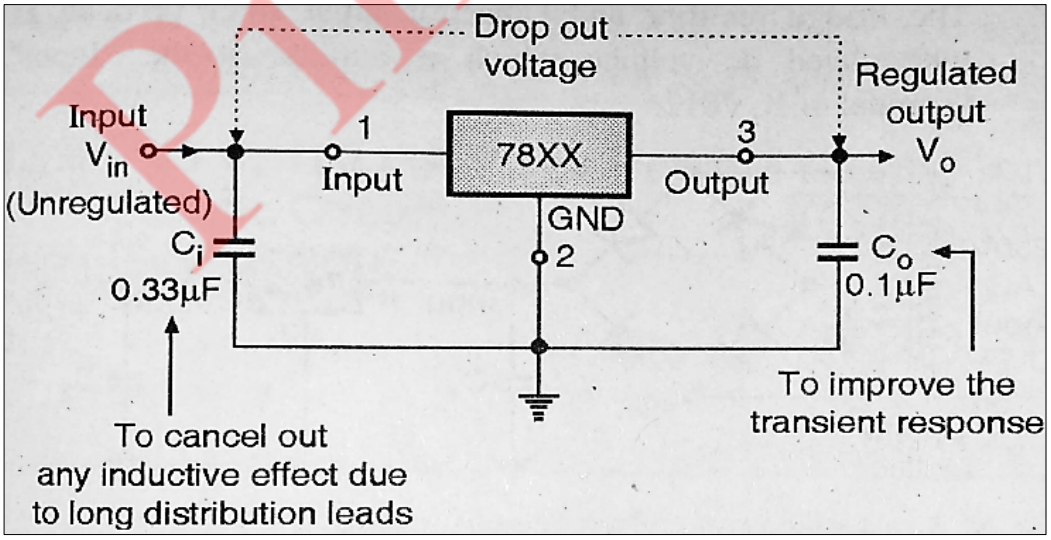


Fig.2 three pin fixed positive regulator IC



Standard connections for three pin fixed IC regulator

The capacitor "C_i" connected between the input terminal and ground cancels out any inductive effect due to long distribution leads.
The output capacitor C_o is used for improving the transient response of the regulator IC. i.e. the response of the regulator to the sudden changes in load.

This capacitor is also helpful in reducing the noise present at the output.
The difference between the unregulated input voltage V_{in} and the output voltage V_o is called as drop out voltage.
Drop out voltage = $V_{in} - V_{out}$
The drop out voltage needs to be at least 2 Volts under all the operating conditions for proper operation of the regulator.

79XX Series (Fixed Negative Voltage Regulator):
A 79XX series is also available in the three-pin fixed voltage category. This series or regulator ICs has been designed to provide a fixed negative output voltage.
These ICs can provide -5, -6, -8, -12, - 15, -18 and -24 V output voltages like the 78XX series.
In addition to that this series provides - 2V and - 5.2 V output voltage options. lists the different negative regulator ICs in 79XX series.

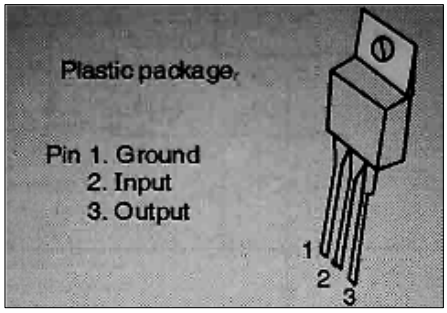
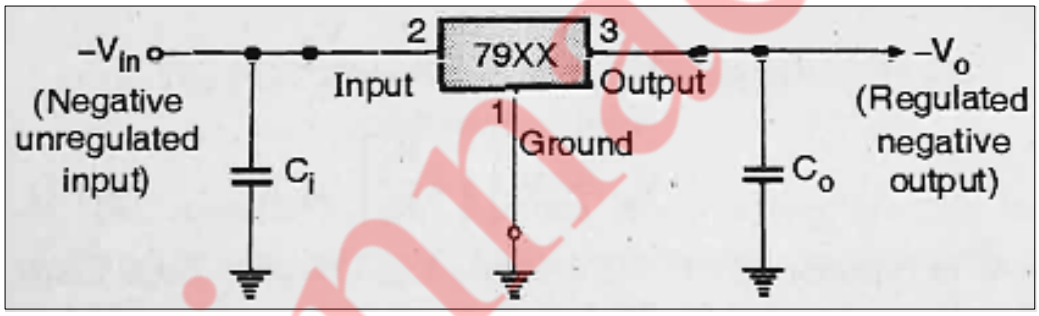


Fig.2 three pin fixed negative regulator IC

IC No.	7905	7906	7908	7912	7915	7918	7924
Output voltage	-5V	-6V	-8V	-12V	-15V	-18V	-24V

Both these voltage regulators ICs are available in two types of packages i.e. TO-3 type metal package and TO-220 type plastic package.
TO-3 package is suitable for the higher power dissipation capability.

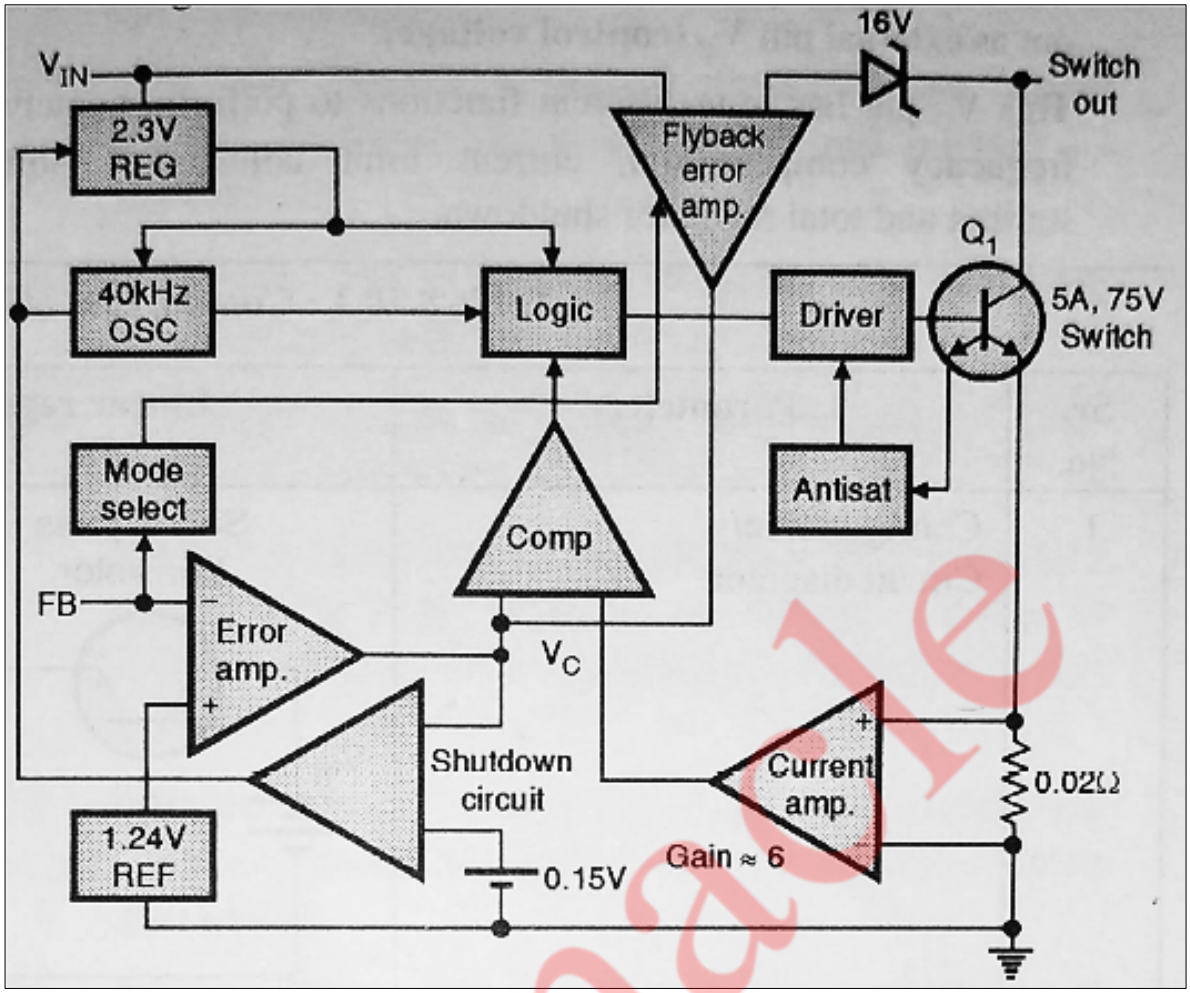


Typical connections of 79XX series

Note: **the order of the terminals of 79XX is not same as that for the 78XX series**.
The role of Ci and Co is same as that discussed for 78XX regulator. The operation of 79XX voltage regulators is exactly same as that of 78XX voltage regulators discussed earlier.

(c) Monolithic switching regulator. **5M**

Ans.



Internal block diagram of LT 1070

LT 1070 is a current mode switching regulator. The duty cycle of the switch (Q1) is directly controlled by sensing the switch current and not by sensing the output voltage.

The switch Q1 is turned on at the beginning of each oscillator cycle. The switch current starts flowing which is continuously sensed by the 0.020 resistance. As soon as the switch current crosses a predetermined level, the switch (Q1) will be turned off.

The current trip level (current at which Q1 is turned off) is set by the control voltage Vc which is obtained at the output of error amplifier

A low drop out internal voltage regulator provides a 2.3 V supply for all the internal blocks of LT 1070. Due to this arrangement the input voltage is allowed to vary over a wide range (3 v to 60 V) without any change m the device performance.

The 40 kHz oscillator shown in Fig. 8.19.2 acts as the basic c1ock for all the internal timing. It turns ON the output switch via the logic and driver circuitry.

The adaptive **antisat (anti-saturation)** circuit will detect the

beginning of saturation of the power switch and automatically adjusts its drive current to limit switch saturation. This helps in minimizing the power dissipation and provides very fast turn off of the power switch.

The 1.2V bandgap reference biases the positive input of the error amplifier as shown in Fig. The negative input of error amplifier is brought out as **FB (feedback)** terminal and used for sensing the output voltage.

There is another function of **FB (feedback)** pin. If this input is connected to ground via an external resistance, then LT 1070 shuts off the main error amplifier and connects the output of the Flyback amplifier directly to the comparator input. LT 1070 will then regulate the value of the Flyback pulse with respect to the supply voltage.

The Flyback pulse is directly proportional to the output voltage in a conventional Flyback converter (transformer coupled). But here we regulate the amplitude of Flyback pulse
to regulate the output with no direct connection between input and output. It is possible to obtain multiple floating outputs.
The error signal produced at the comparator input is brought out as external pin Vc (control voltage).
This Vc pin has four different functions to perform, namely frequency compensation, current limit adjustment, soft starting and total regulator shutdown.
During the normal operation of the regulator this pin (Vc) has a voltage between 0.9 V (low output current) and 2.0 V (high output current).
The error amplifiers are current output (gm) types. So, this voltage can be externally clamped for adjusting the current limit.
Similarly, soft start could be provided with the help of a capacitor coupled external clamp.
If Vc = 0 (V c pin connected to ground through a diode) then the switch duty cycle will be equal to zero and LT 1070 is placed in an idle mode.
Pulling V c pin below 0.15 V will cause a total shutdown of the regulator IC LT 1070. In that case this IC draws only 50 µA current from the DC supply.

Features:

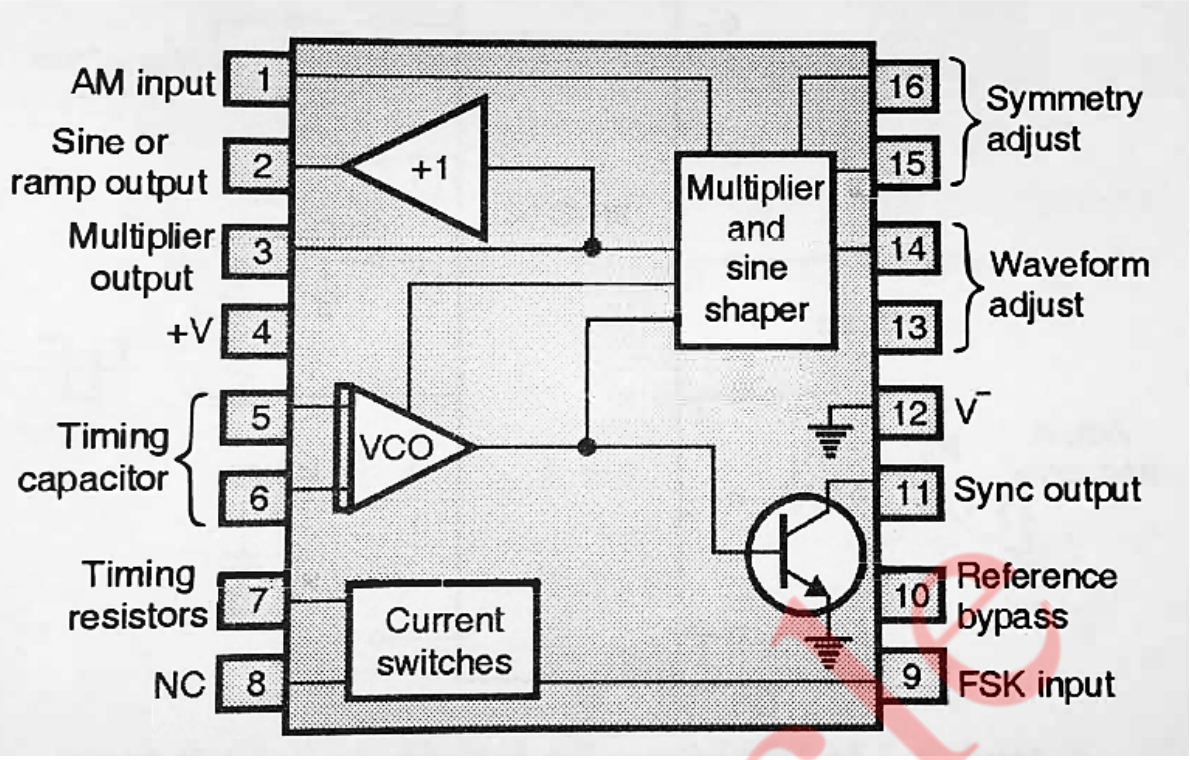
- Wide input voltage range: 3 V to 60 V.
- Low quiescent current: 6 mA.
- Internal 5 A switch (2.5 A for LT 1071).
- Very few external parts required.
- Self-protected against overloads.
- Operates in nearly all switching topologies.
- Shutdown mode needs 50 µA supply current only.
- Flyback regulated mode has fully floating outputs.
- Comes in standard 5-pin TO-220 package.
- Can be externally synchronized.

Applications of LT 1070:

- Logic supply 5 V to 1 OA.
- 5 V logic to± 15 V op amp supply.
- Off-line converter up to 200 W.
- Battery upconverter.
- Power inverter (+ to-) or (-to +).
- Fully floating multiple outputs are available.
- For lower current applications, see the LT 1072.

(d) XR2206 waveform generator. **5M**

Ans.



functional block diagram and pin connection diagram

This is another important waveform generator JC. This IC is capable of producing a sinewave or ramp outputs. The multiplier output is also made available to the user a1ongwith the symmetry adjustment.

This function generator also consists of a logarithmic wave shaper to convert the triangular wave to the sine wave.

For generating the triangular and square wave an emitter coupled VCO is employed.

Description of the functional block diagram:

The heart of this IC is the voltage-controlled oscillator (VCO), which is driven via a pair of current switches. The VCO capacitor or timing capacitor is externally connected between pins 5 and 6.

The VCO timing resistor is connected between pin no. 7 and GND.

The external capacitor connected between pins 5 and 6 and the timing resistor will decide the output frequency.

VCO produces two waveforms simultaneously. One of them is a linear ramp which is fed to the multiplier and sine shaper. And the other output is a rectangular waveform which is applied to pin no. l 1 via the internal transistor.

Ramp output is applied to the multiplier and sine shaper block. This block acts as an amplifier with controlled gain. It gives a high impedance output at pin 3 and a 600 Q buffered output at pin no. 2.

The distortion in the sinewave output can be adjusted to a very low value (typically 0.5%).

The gain and output phase of the multiplier can be changed by applying a dc bias or ac signal to pin1 of the IC.

The output changes linearly with change in voltage at pin no.1. This can be used to amplitude modulate the outputs of the IC at pins 2 and 3.

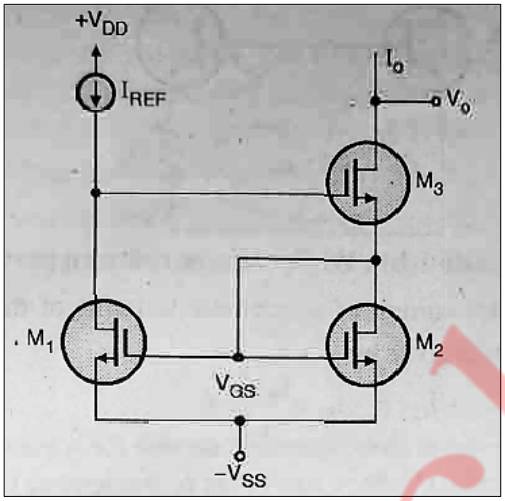
(e) Wilson current source. **5M**

Ans. The basic Wilson current mirror using MOSFETs is as shown in Fig.(a)

The V_{DS} values of M1 and M2 in this circuit are not equal to each other. Also, $\lambda \neq 0$. Hence the ratio of I_O and I_{REF} is slightly different from the aspect ratios.

the MOS version of Wilson current mirror. The MOS Wilson mirror has a higher value of R_O as compared to that of the bipolar Wilson mirror.

The basic structure and principle of operation of the Wilson MOS mirror is same as that of the BJT Wilson mirror.



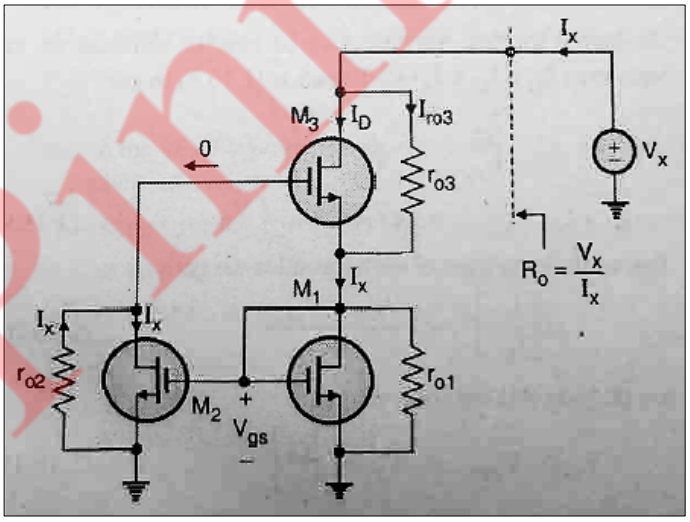
The Wilson MOS mirror fig.(a)

Output resistance (Ro):

for the small signal analysis of this circuit. It can be shown from the circuit of Fig.(b) that the output resistance R0 of the Wilson current mirror is

approximately equal to, $R_O \cong g_{m3}\, r_{o3}\, r_{o2}$

As can be seen, this value is same as the output resistance of the cascode current mirror circuit.



Analysis to determine the output resistance fig.(b)

Advantages of Wilson current source:

1.High output resistance.

2.Low sensitivity to the MOS transistor currents and variations in transistor parameters.

Disadvantages of Wilson current source:

While designing the current source circuits the main problems encountered are:

1.Mismatching among the MOS transistors.

2.Effect of variation in the power supply voltage.

3.Effect of variation in temperature.